

# Qualitative Analysis of 3D Routing Algorithms in 3×3×3 Mesh NoC Topology Under Varying Load in Bio-SoC

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## ABSTRACT

This article presents a qualitative analysis of a 3D routing algorithm in a 3×3×3 mesh NOC topology. The effect of load variation on throughput, total energy, and maximum delay for different types of routing is observed. The simulation was performed on an Access NOXIM network-on-chip simulator under random traffic conditions. The research involves quality parameters like total packets received, total received flits, global average delay (cycles), global average throughput (flits/cycle), throughput (flits/cycle/IP), max delay (cycles), total energy (J), average power (J/cycle), average power per router (J/cycle), and average waiting time in each buffer. In this article, it was observed after comparing all the routing techniques against the mention parameters the XYZ routing techniques was found perform better followed by West first, and North last, while poor performance was observed against odd-even, negative first, and fully adaptive.

## KEYWORDS

3D-Mesh, E-Hospital, Energy, Network-On-Chip, NOXIM, Routing, Throughput

## 1. INTRODUCTION

A fast and smart biomedical DAS is composed of many integrated IPs and scaled interconnects. Many smart sensors are either integrated within the chip in the form of an IP block or connected through the smart interface. The logged data is communicated through internet enabled integrated IP. The multilayer 3D system on chip is the best on-chip clinic solution, Where the sensing row is for getting the data from various biomedical sensors, the middle row is to log the data and generate the actuating signals for remote surgery through robotic hands. The last layer of the architecture contains the set of IP cores of outer actuators interface through the internet, Bluetooth and wi-fi modules. The scaled SoC architecture for biomedical applications is very crucial for real time applications. So, the routing algorithms should route the packets with improved quality of services. Expansion of new ports in the router can vanquish issue of obliged data transfer capacity and scaling. 3D NoC, architecture created using various uniform silicon planes and each unique plane is a 2D mesh topology associated with vertical connections or interconnection wires. A capable routing is required to explore all the available approaches to streamline the performance as far as throughput, number of received packets, received flits, latency, energy and average power (Saini & Ahmed, 2015; Kourdy & Nouri, 2012). NoC configuration must be basic and short-way route is very considered for low inertness and power dispersal. another option to traditional on-chip correspondence coordinate with a uniform stackable multi-chip modules (MCM) in three-dimensional utilizing through silicon via (TSV). The

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change from 2D to 3D NoC is done by appropriating the tiles on to different layers of 3D NoC. (Paulo & Ababei, 2010) Explained outline of homogeneous framework on particular layers using heterogeneous floor plan (Sehgal, 2015). The router assignment-based plan approach is utilized for arrangement of Processing Elements (PE) on first layers and their limited association with the router is determined to the second layer. Application particular NoC plan with upgraded control utilization and least range managed rip up and reroute technique for coordinating streams and a router blending framework to streamline a given framework (Yan & Lin, 2011). NoC architecture gives a wide arrangement space including system topology, routing algorithms, and router design, where all impact framework execution to the impairment of different measures of system assets; along these lines the system design for such installed applications ought to be carefully chosen to meet the prerequisites (Matsutani, Koibuchi, & Amano, 2007). Such implanted applications frequently request tight outline imperatives regarding cost and performance, in this manner the silicon spending plan accessible for their on-chip mastermind structure should be unassuming as long as the required execution is met. System on-Chips (SoCs) have been concentrated to interface various processing cores on a solitary chip by acquainting a system structure comparable with that of parallel PCs (Dally & Towles, 2001) Other than NoCs, three-dimensional incorporated circuits (3D ICs) are another appealing answer for framework performance change by decreasing the interconnect length. (Beyne, 2006) However a noteworthy new worldview for proceeded with Moore's law incorporation is 3D chip stacks in light of an assortment of vertical interconnection techniques (Ye, Duan, Xu et al., 2009). 3D integration gives chances to cost diminishment and yield change in reconciliation of various advancements, for example, CMOS, DRAM and MEMS circuits through the capacity to actualize them over multiple die layers on a similar chip. It can likewise decrease shape factor in applications where estimate is basic, while powerful warmth dispersal and temperature control can be a test. To get the most preferred standpoint out of 3D chip stacks in multiprocessor systems, the correspondence configuration needs to help beneficial and high throughput vertical communication.

In this paper, we analyze the adaptability of the NoC for such frameworks. Moreover, the developing three-dimensional (3D) reconciliation and process advances permit the plan of multi-level Integrated Circuits (ICs). As outlined in (Vasilis & Friedman, 2007), this makes new plan openings in NoC outline. With a specific end goal to fulfill the requests of rising frameworks for scaling, execution and usefulness 3D incorporation is away to suit these requests (9). For example, a critical lessening can be proficient in the number and length of overall interconnection using 3-D integration. On choosing whether to pick a two-dimensional (2D) or 3D NoC as a plan it is showed up in (Alexandros B, 2007) that 3D NoCs are profitable, giving better execution.

## 2. RELATED WORK

Many researchers have used the NoC with biomedical enabled IPs for real-time analysis of biomedical and biometric signals (Al Khatib et al., 2006). NoC offer high adaptability and the consistency of a system structure, supporting less troublesome interconnect showing and all the more intense circuits. The standard interconnect spine of the system joined with proper communication protocols improve the adaptability of such frameworks. The benefits of 3D NoC have been now talked about before. Because of the need of expanding adaptability in structure what's more, ultra-high speed for applications, for example, real time video handling, multimedia, consumer, etc. Beginning sequentially with the work that has contributed its part of research and framing base for this paper. Ogras, Hu, and Marculescu (2005) had called attention to that identification of information packets and errors in routing. An autonomous body sensor network can easily be mapped on 3D NoC, where each layer is assigned for sensing logging and actuating (Wang et al., 2010). The proposed strategy depends on new error detection and correction component appropriate for dynamic NOCs, where the number and position of processor components shift during runtime. This paper gives the traffic load variations on average latency and power for DYAD routing calculation, this calculation having both deterministic

and versatile routing calculation. This calculation is utilized to decide the way of a packets from source to the destination. The best exhibitions of routing calculation in the NOC designs are least latency, least power and greatest throughput. The point is to decrease the transmission delay and to guarantee the need to the shortest way routing of information. (Rahmani, Latif, Liljeberg et al., 2010) presents that the conventional bus-based system frameworks are not reliable for SOC due to absence of adaptability, parallelism incorporation, high inactivity, control diffusing, and low throughput. System on chip has been found as a promising answer for future frameworks on chip outline and is in its condition-of-workmanship of NoC. It offers more versatility than the common transport-based interconnection, enables more processors to work simultaneously. 3D NoC has been proposed to manage the issues experienced in 2D NoC. This offers arrangement of bring down power utilization and higher speed. In this manner, a  $2 \times 2 \times 4$  mesh topology virtual channel switch is being composed, Simulated and Synthesized in Xilinx ISE plan suite. (Khan & Ansari, 2011) proposed the quadrant XYZ routing algorithm is used to build a 3D Asymmetric Torus NoC router. Because of these types of networks has steady hub degree, recursive structure, great scalability and basic communication algorithms. Paper introduces a Register Transfer Logic (RTL) reproduction model of Quadrant-XYZ measurement arrange routing algorithm for 3-D asymmetric torus NoC written in Verilog and synthesize on Xilinx vertex-6 achieved maximum operating frequency 750MHz. (Feero & Pande, 2009) Three-dimensional NoCs are common expansions of 2D plans. this paper, shown that other than decreasing the impression in a created plan, 3D arranges structures give a superior execution contrasted with customary, 2D NoC designs. Author illustrated that both mesh and tree-based NoCs are prepared to do accomplishing better execution when instantiated in a 3D IC condition contrasted and more standard 2D utilization condition. The mesh-based models demonstrate huge execution picks up as far as throughput, inertness, and power dispersal with a little zone overhead. Then again, the, 3D tree-based NoCs accomplish critical pick up in power dispersal and area overhead with no change in throughput and latency. With the appearance of 3D ICs, the achievable execution profits by NoC approach will be more articulated as appeared in this paper. Thusly, this will encourage selection of the NoC demonstrate as a standard (Dally & Towles, 2001) looked at 2D MESH structures and their 3D partners by investigating the zero-stack latency and power utilization of each system. This is an assessment that demonstrates a portion of the benefits of 3D NoCs, yet it not one or the other applies any real-time activity design nor does it gauge other important execution measurements. We plan to address these worries by applying continuous activity outlines in a cycle-correct simulation and by measuring execution through built up measurements for 3D NoC structures (Ahmed & Abdallah, 2013). The paper exhibits the performance examination of routing techniques on  $3 \times 3$  mesh NOC topology. The impact of load on delay and total network energy for different types of routing is observed. The reproduction is performed on NOXIM organize on chip test system under random traffic conditions. The exploration includes creating of arrangement model based on support vector machine. The quality parameters gave as contribution to the model against the execution for routing algorithms in view of Network-on-Chip stage are minimum delay, least vitality and greatest throughput.

### 3. 3D NOC EVALUATION MODEL

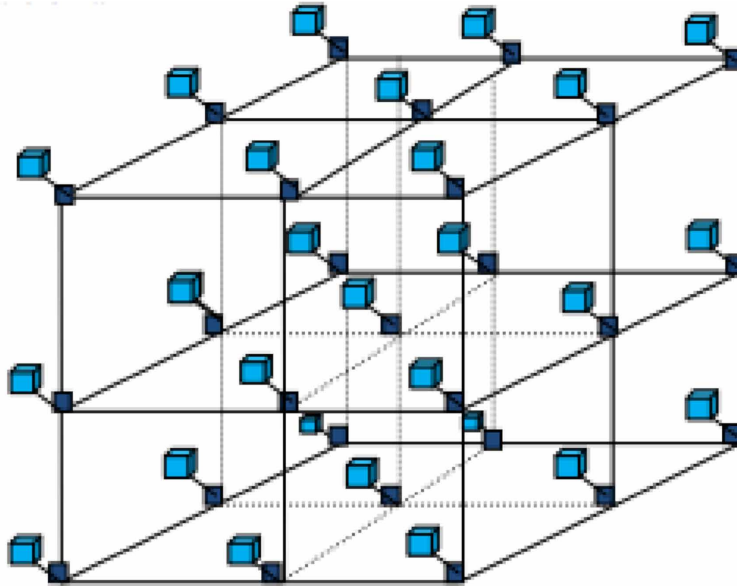
The comparison of 3D routing algorithm in  $3 \times 3 \times 3$  mesh network on chip topology as shown in Figure 1 is carried out Noxim Simulator.

Link Calculation:

$$XL = X1 \times X2 \times (N3-1) + X1 \times X3 \times (N2-1) + X2 \times X3 \times (N3-1)$$

Where XL is total number of links

Figure 1. 3×3×3 mesh network topology



X1 = X Dimension  
X2 = Y Dimension  
X1 = Z Dimension

The qualitative analysis involved the parameter including Total Packet Received (TPR), Total received flits(TRF), Global average delay(cycles) (GAD), Global average throughput (flits/cycle) (GAT), Throughput (flits/cycle/IP)(T), Max delay (cycles)(MD), Total energy (J)(TE), Avg power (J/cycle)(AP), Avg power per router (J/cycle)(APPR), Avg waiting time in each buffer (cycles)(AWT) as shown in Table 1. The analysis was done under varying load condition included by packet injection ratio having range from 0.1 to 1.0 means that each node sends packets to this node during a cycle having period value 1000. The output generated is shared in data file for each routing algorithm under varying packet injection ratio. The data

generated was used to compute correlation score by the correlation model as shown in Figure 2. The correlation plot among 3D routing algorithm based on the parameters including throughput(T), Total received packets, Total received flits, Global average delay, Global average throughput, Max delay and Total energy shown a positive correlation of (1) between XYZ, north last and negative first. The value involves < 1 for odd even and fully adaptive 0 routing algorithms. Although all the 3D routing algorithms have shown a positive correlation with XYZ routing and with a slightly varying correlation sure. The high positive correlation proves all the routing algorithms to behave in a similar fashion against the input parameters but with varying efficiency as shown in Figure 2.

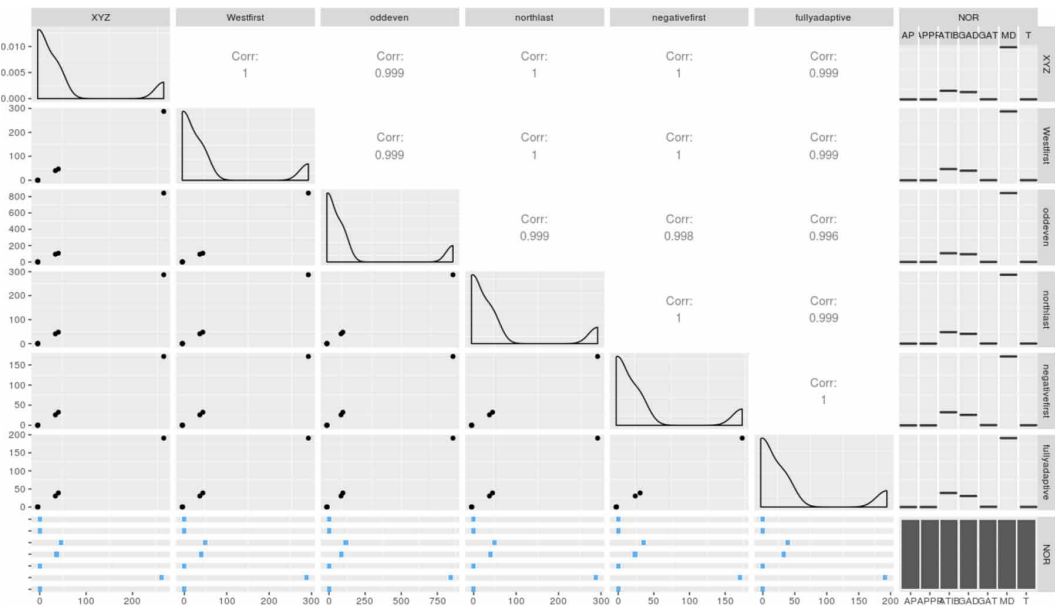
## 2.1 Total Packet Received

Total packet Received of XYZ routing was observed maximum value 27371 and Negative first routing was observed minimum value 2300 (Table 2). Under varying load conditions where packet injection ratio were varied from 0.1 to 1.0 as shown in Figure 3.

**Table 1. Average values of all routing algorithms**

	TRF	TRF	GAD	GAT	T	MD	TE	AP	APPR	AWTB
Name of routing	Total received packets	Total received flits	Global average delay	Global average throughput	Throughput	Max delay	Total energy	Avg power	Avg power per router	Avg waiting time in each buffer
XYZ	17794.5	142309.7	36.99745	0.42841	0.395344	292.2	0.005334	5.33E-07	1.48E-08	43.21712
Westfirst	17514.6	140074.2	40.39419	0.424003	0.389134	319.1	0.005256	5.26E-07	1.46E-08	47.0513
oddeven	13831.7	110607.3	91.86806	0.342039	0.307273	961.3	0.004154	4.15E-07	1.15E-08	104.0377
northlast	17434.2	139431.1	41.83271	0.41877	0.387347	291.6	0.005233	5.23E-07	1.45E-08	48.63043
negativefirst	10474	83767.2	25.60681	0.548094	0.23271	172.7	0.003175	3.18E-07	8.82E-09	31.49928
fullyadaptive	10859.9	86850.8	31.59711	0.509291	0.241276	181.1	0.003294	3.29E-07	9.15E-09	39.98067

**Figure 2. Correlation score by the correlation model**



## 2.2 Total Received Flits

A total Received flit of XYZ routing was observed maximum value 218903 and Negative first routing was observed minimum value 18400 (Table 3). Under varying load conditions where packet injection ratio was varied from 0.1 to 1.0 as shown in Figure 4

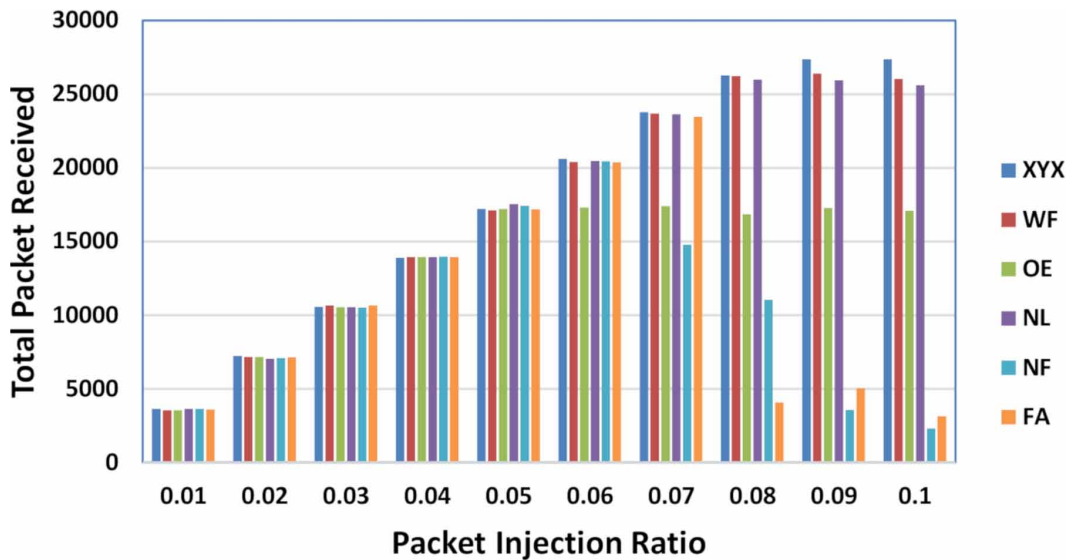
## 2.3 Global Average Delay

Global Average Delay of Odd-Even routing was observed maximum value 176.12 and Negative first routing was observed minimum value 51.909. Under varying load conditions where packet injection ratio were varied from 0.1 to 1.0 as shown in figure 5

**Table 2. Total packet received for all routing algorithms**

Routing Techniques	XYZ	WF	OE	NL	NF	FA
PIR						
0.01	3637	3540	3547	3627	3635	3589
0.02	7232	7150	7169	7033	7086	7137
0.03	10574	10664	10546	10532	10516	10659
0.04	13893	13953	13939	13952	13975	13937
0.05	17197	17102	17205	17536	17421	17179
0.06	20602	20394	17296	20469	20437	20382
0.07	23789	23686	17402	23638	14776	23470
0.08	26282	26225	16856	25993	11041	4072
0.09	27368	26395	17279	25956	3553	5049
0.1	27371	26037	17078	25606	2300	3125

**Figure 3. Total packet received**



## 2.4 Global Average Throughput (Flits/Cycle)

Global Average Throughput of Negative First routing was observed maximum value 1.1432 and Odd-Even routing was observed minimum value 0.411 (Table 5). Under varying load conditions where packet injection ratio were varied from 0.1 to 1.0 as shown in Figure 6

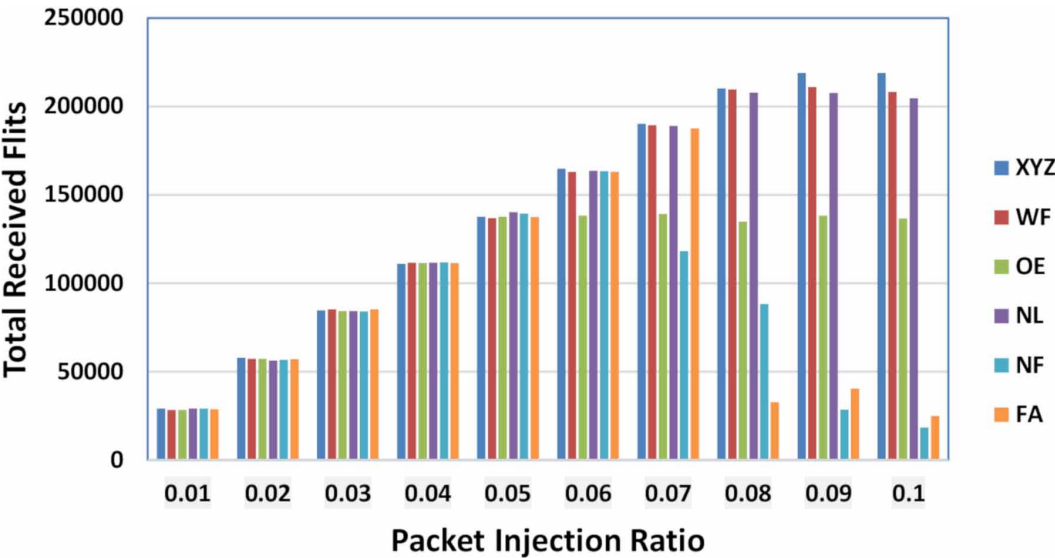
## 2.5 Throughput (flits/cycle/IP)

Throughput of XYZ routing was observed maximum value 0.60812 and Negative First routing was observed minimum value 0.05111 (Table 6). Under varying load conditions where packet injection ratio were varied from 0.1 to 1.0 as shown in Figure 7

Table 3. Total Received flits for all routing algorithms

Routing Techniques	XYZ	WF	OE	NL	NF	FA
PIR						
0.01	29096	28319	28371	29004	29075	28706
0.02	57833	57192	57320	56240	56661	57084
0.03	84566	85289	84325	84227	84078	85255
0.04	111092	111581	111470	111578	111778	111464
0.05	137527	136770	137594	140249	139329	137377
0.06	164778	163095	138318	163698	163446	162984
0.07	190254	189445	139142	189059	118178	187670
0.08	210161	209703	134806	207893	88303	32576
0.09	218887	211095	138171	207573	28424	40392
0.1	218903	208253	136556	204790	18400	25000

Figure 4. Total received flits



## 2.6 Max Delay (Cycles)

Maximum Delay of Odd-Even routing was observed maximum value 1694 and Negative First routing was observed minimum value 243 (Table 7). Under varying load conditions where packet injection ratio was varied from 0.1 to 1.0 as shown in Figure 8

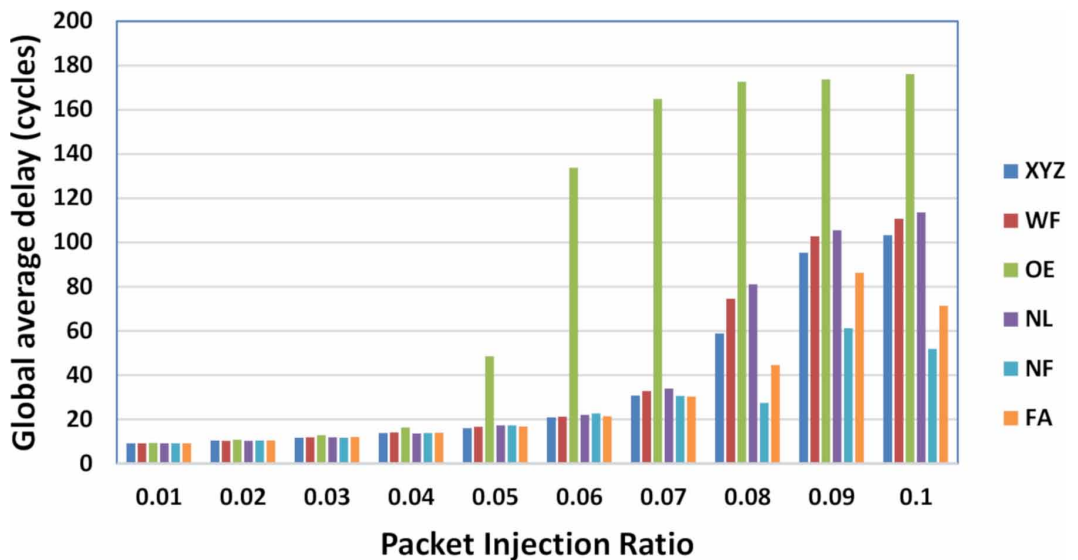
## 2.7 Total energy (J)

Total Energy of XYZ routing was observed maximum value 0.00815734 and Negative First routing was observed minimum value 0.000777265 (Table 8). Under varying load conditions where packet injection ratio was varied from 0.1 to 1.0 as shown in Figure 9.

Table 4. Global average delay for all routing algorithms

Routing Techniques	XYZ	WF	OE	NL	NF	FA
PIR						
0.01	9.168	9.20593	9.31999	9.2214	9.15763	9.18055
0.02	10.3803	10.2761	10.7551	10.3056	10.4445	10.4215
0.03	11.6934	11.8273	12.748	11.85	11.7503	11.9908
0.04	13.7183	14.1114	16.2124	13.6277	13.7698	13.9094
0.05	15.9869	16.5416	48.5791	17.1925	17.2391	16.7104
0.06	20.9276	21.2005	133.778	21.9753	22.714	21.351
0.07	30.7072	32.7534	164.822	33.8543	30.5138	30.3002
0.08	58.7509	74.4877	172.59	81.1273	27.3839	44.5575
0.09	95.3059	102.801	173.756	105.563	61.1855	86.2515
0.1	103.336	110.737	176.12	113.61	51.9096	71.2982

Figure 5. Global average delay



### 3. RESULTS AND DISCUSSION

#### 3.1 Throughput Vs Maximum Delay

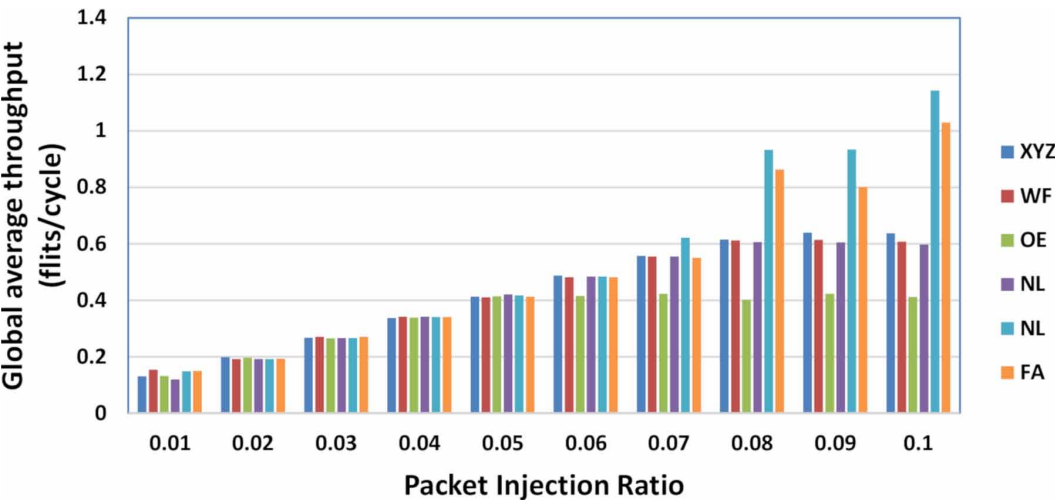
The routing algorithm XYZ was observed to provide maximum throughput having value 0.4 compared to rest. Negative first routing algorithm was observed to provide minimum throughput with value 0.23. While maximum delay with respect to high throughput was also observed in case of XYZ routing having value 0.15. The minimum value for maximum delay with respect to throughput was observed with value  $< 0.1$  in case of odd even routing algorithm. Although in rest of routing algorithm maximum delay was observed to be between  $> 0.1$  and  $< 0.16$  but XYZ outperformed all the other routing algorithms in the comparison as shown in Figure 10



Table 5. Global average throughput for all routing algorithms

Routing Techniques	XYZ	WF	OE	NL	NF	FA
PIR						
0.01	0.131128	0.154169	0.13191	0.119436	0.148654	0.149621
0.02	0.198621	0.191864	0.19651	0.19231	0.191901	0.193352
0.03	0.267713	0.270714	0.265213	0.265825	0.266166	0.270911
0.04	0.337168	0.342166	0.33883	0.341971	0.341099	0.341031
0.05	0.412397	0.410307	0.413886	0.420509	0.417601	0.412882
0.06	0.487191	0.481751	0.415591	0.484218	0.48367	0.482091
0.07	0.557182	0.555164	0.422513	0.554968	0.621943	0.550318
0.08	0.614705	0.61205	0.401513	0.605731	0.932598	0.862763
0.09	0.640138	0.614538	0.422819	0.605337	0.934038	0.800862
0.1	0.637857	0.60731	0.411604	0.597396	1.14327	1.02908

Figure 6. Global average throughput



### 3.2 Throughput Vs Total energy

The energy consumption is one of the important criteria while comparing routing in 3D NoC mesh networks. Although maximum energy with respect to throughput observed against the all routing algorithms was  $>0.7$ (scaled). The throughput was obtained high only in case of XYZ while minimum throughput was observed in case of negative first followed by fully adaptive routing algorithm as shown in Figure 11.

#### 3.3 Distribution Analysis

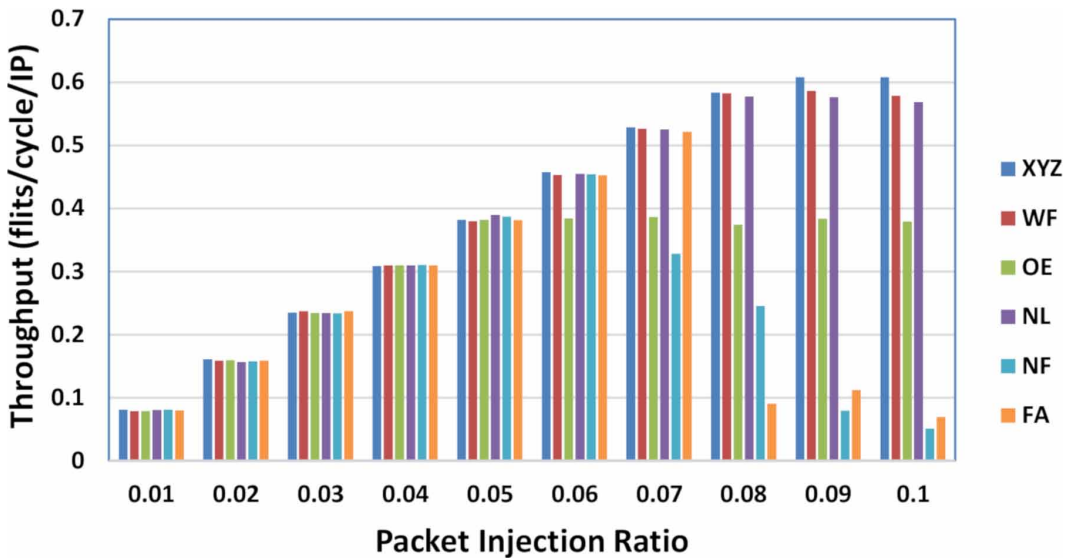
The distribution analysis was used to compute the distribution analysis based on three important parameters as shown in Table 9.

The XYZ was observed to perform much better in terms of throughput, delay and energy consumed compared to rest. Through energy consumed by each routing algorithm under varying load almost

Table 6. Throughput for all routing algorithms

Routing Techniques	XYZ	WF	OE	NL	NF	FA
PIR						
<b>0.01</b>	0.08083	0.078672	0.078816	0.080575	0.080772	0.079747
<b>0.02</b>	0.160663	0.158883	0.159238	0.156238	0.157407	0.158583
<b>0.03</b>	0.234929	0.236938	0.23426	0.233987	0.233573	0.236843
<b>0.04</b>	0.30862	0.309978	0.30967	0.30997	0.310525	0.309653
<b>0.05</b>	0.382058	0.379955	0.382244	0.38962	0.387064	0.381641
<b>0.06</b>	0.457762	0.453087	0.384255	0.454762	0.454062	0.452779
<b>0.07</b>	0.528536	0.526289	0.386544	0.525216	0.328305	0.521358
<b>0.08</b>	0.583839	0.582567	0.374499	0.577538	0.245311	0.090498
<b>0.09</b>	0.60808	0.586434	0.383847	0.576649	0.078964	0.112211
<b>0.1</b>	0.608125	0.578538	0.37936	0.568918	0.051116	0.069451

Figure 7. Throughput



similar against each algorithm but XYZ was observed to have best throughput vs delay ratio as seen in the Figure 12 compared to rest. The performance of odd even, fully adaptive and negative first routing algorithm was found to be worst shown in Table 9

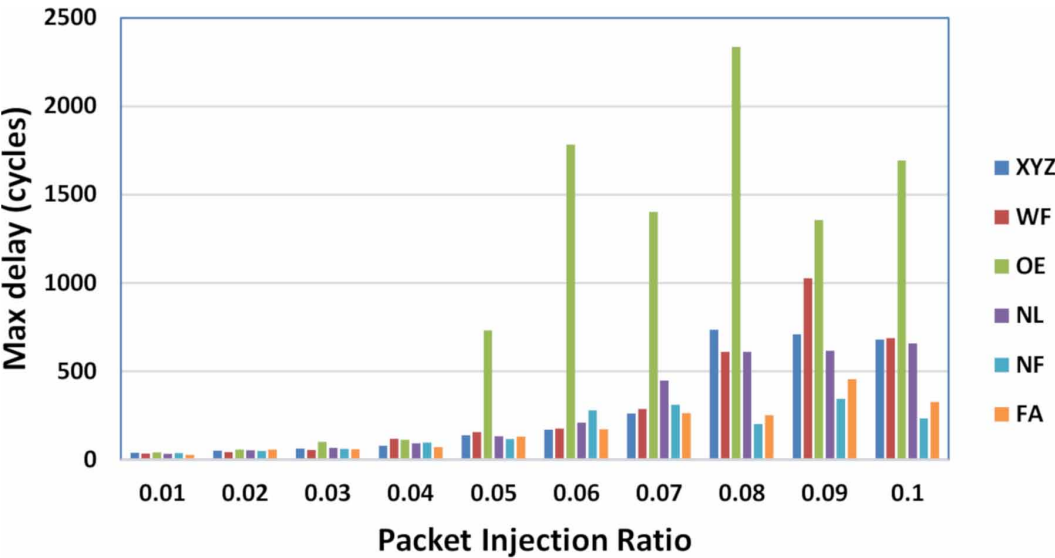
#### 4. CONCLUSION AND FUTURE SCOPE

In the simulation using 3D NoC mesh analytical model it was conformed that the performance of XYZ was found to be better when compared to the rest other west first, odd even north last, negative first and fully adaptive. While the performance of west first, odd even and north last routing algorithm was observed to be average. The poor performance in terms of throughput and delay was observed

Table 7. Max delay for all routing algorithms

Routing Techniques	XYZ	WF	OE	NL	NF	FA
PIR						
0.01	39	34	40	32	36	27
0.02	50	42	56	53	49	56
0.03	62	54	101	66	60	59
0.04	78	119	113	92	97	70
0.05	138	155	731	132	116	130
0.06	169	176	1783	209	279	172
0.07	261	286	1403	447	311	264
0.08	736	610	2336	611	201	251
0.09	709	1027	1356	617	344	456
0.1	680	688	1694	657	234	326

Figure 8. Max delay



in negative first and fully adaptive. The best implementation of proposed work is Clinic-on-Chip as shown in Figure 13.

The paper has investigated the mentioned routing algorithms for 3D mesh topology in network-on-chip. The intent of the study was to determine the best performance among the compared routing algorithms in term of quality parameters as shown in table1. It has been observed that XYZ routing algorithm which tries to find the nearest route with respect to X, Y, Z directions towards the destination out performance the rest of the algorithms. In the future work we may go for multilevel congestion analysis in other to analyze and future improves the performance of XYZ algorithms.

Table 8. Total energy for all routing algorithms

Routing Techniques	XYZ	WF	OE	NL	NF	FA
PIR						
0.01	0.001158	0.00113	0.001121	0.001146	0.001148	0.001142
0.02	0.002221	0.002196	0.00219	0.002153	0.002174	0.002185
0.03	0.003206	0.003226	0.003192	0.003194	0.003177	0.003218
0.04	0.004179	0.004215	0.004191	0.004192	0.004187	0.004211
0.05	0.005145	0.005127	0.005127	0.005237	0.005226	0.005154
0.06	0.006142	0.006091	0.005175	0.006113	0.006129	0.006105
0.07	0.007115	0.007037	0.00524	0.007077	0.004436	0.006989
0.08	0.007845	0.007827	0.005021	0.007771	0.003351	0.001309
0.09	0.008174	0.00791	0.00516	0.007775	0.001147	0.001597
0.1	0.008157	0.007797	0.005118	0.007674	0.000777	0.001033

Figure 9. Total energy

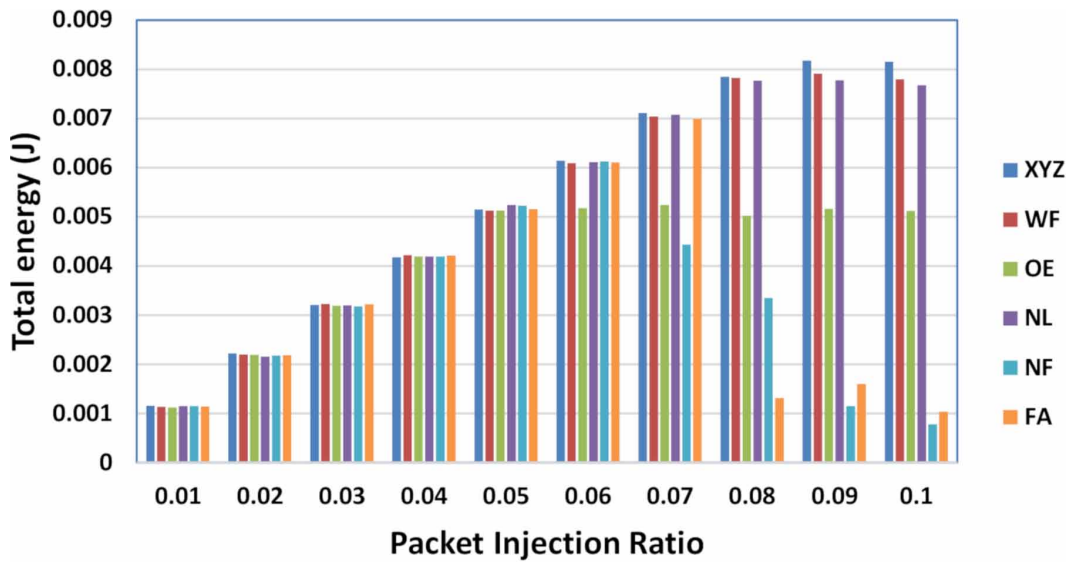


Figure 10. Throughput vs. maximum delay

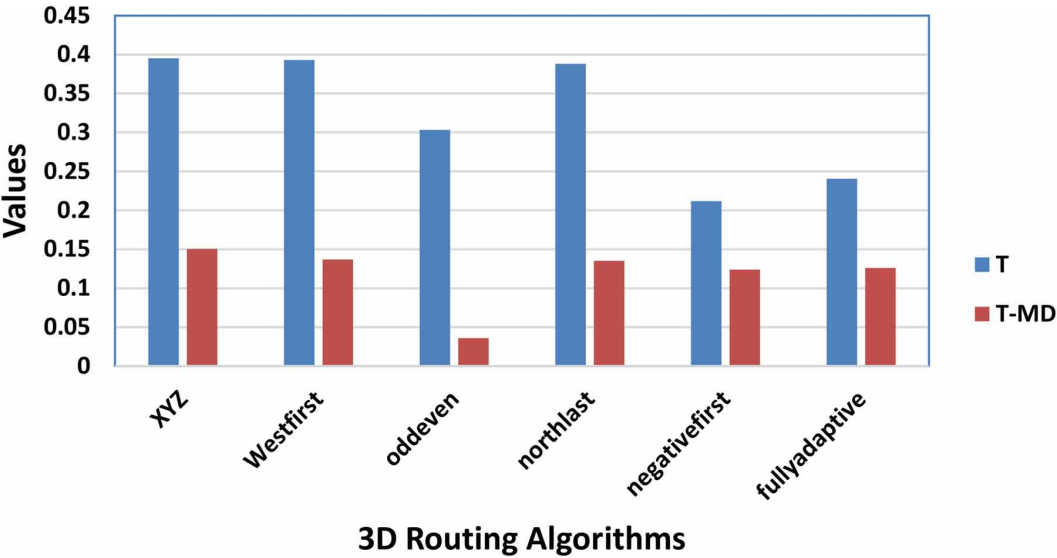
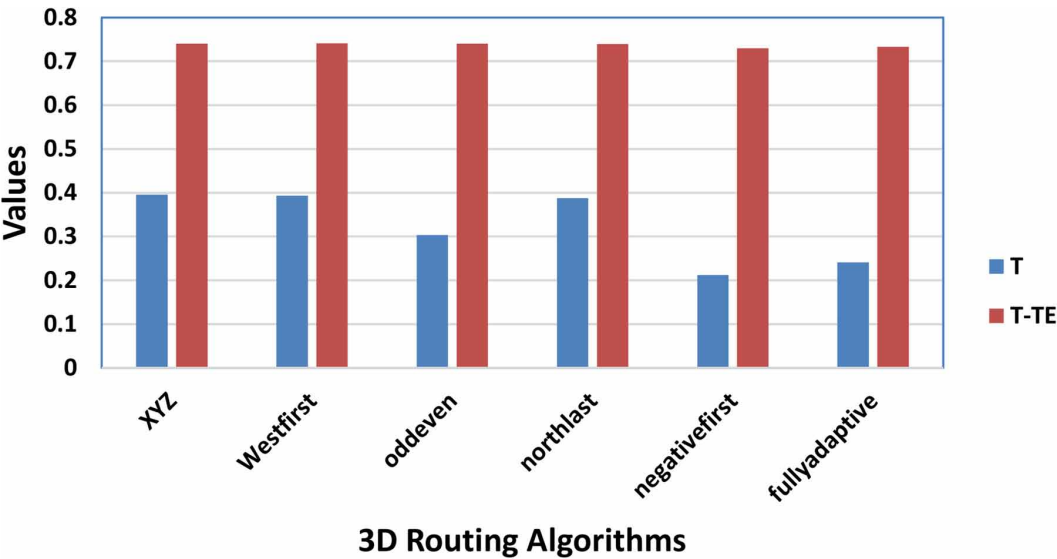


Figure 11. Throughput vs total energy



**Table 9. Throughput vs total energy and throughput vs maximum delay**

Name of routing	Throughput	Total energy	Max delay	Throughput vs total energy (T-STE)	Throughput vs max delay (T-MD)
XYZ	0.395344	0.005336	262.9	0.7408	0.150378178
Westfirst	0.393148	0.005307	287.6	0.7409	0.136699583
oddeven	0.303455	0.004099	843.6	0.7403	0.035971432
northlast	0.387885	0.005247	287	0.7393	0.135151533
negativefirst	0.211896	0.002902	171	0.7302	0.123915556
fullyadaptive	0.240607	0.003282	190.8	0.733	0.126104507

**Figure 12. Distribution analysis**

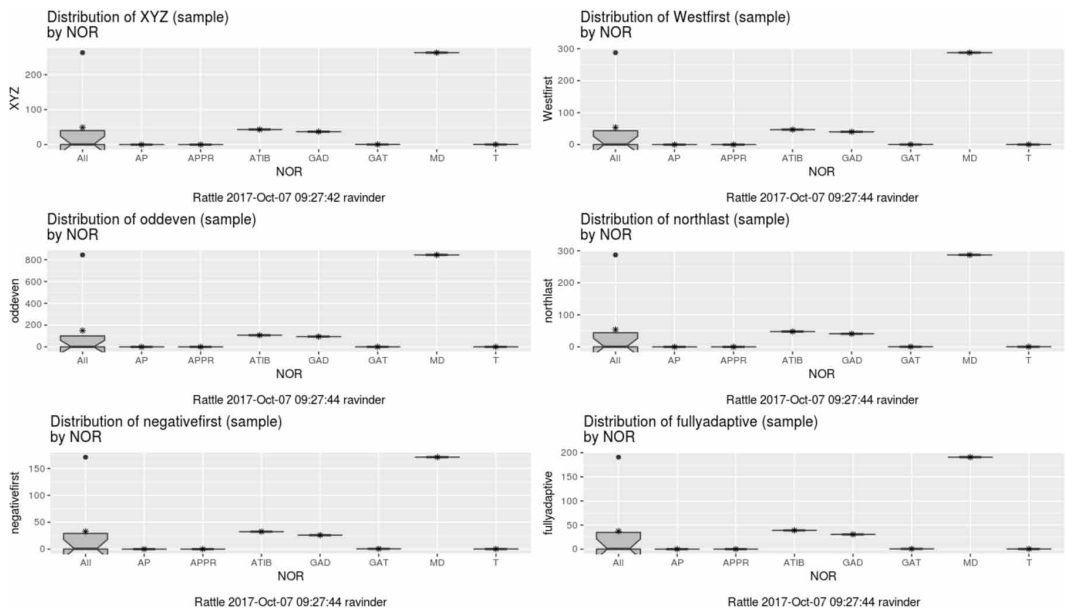
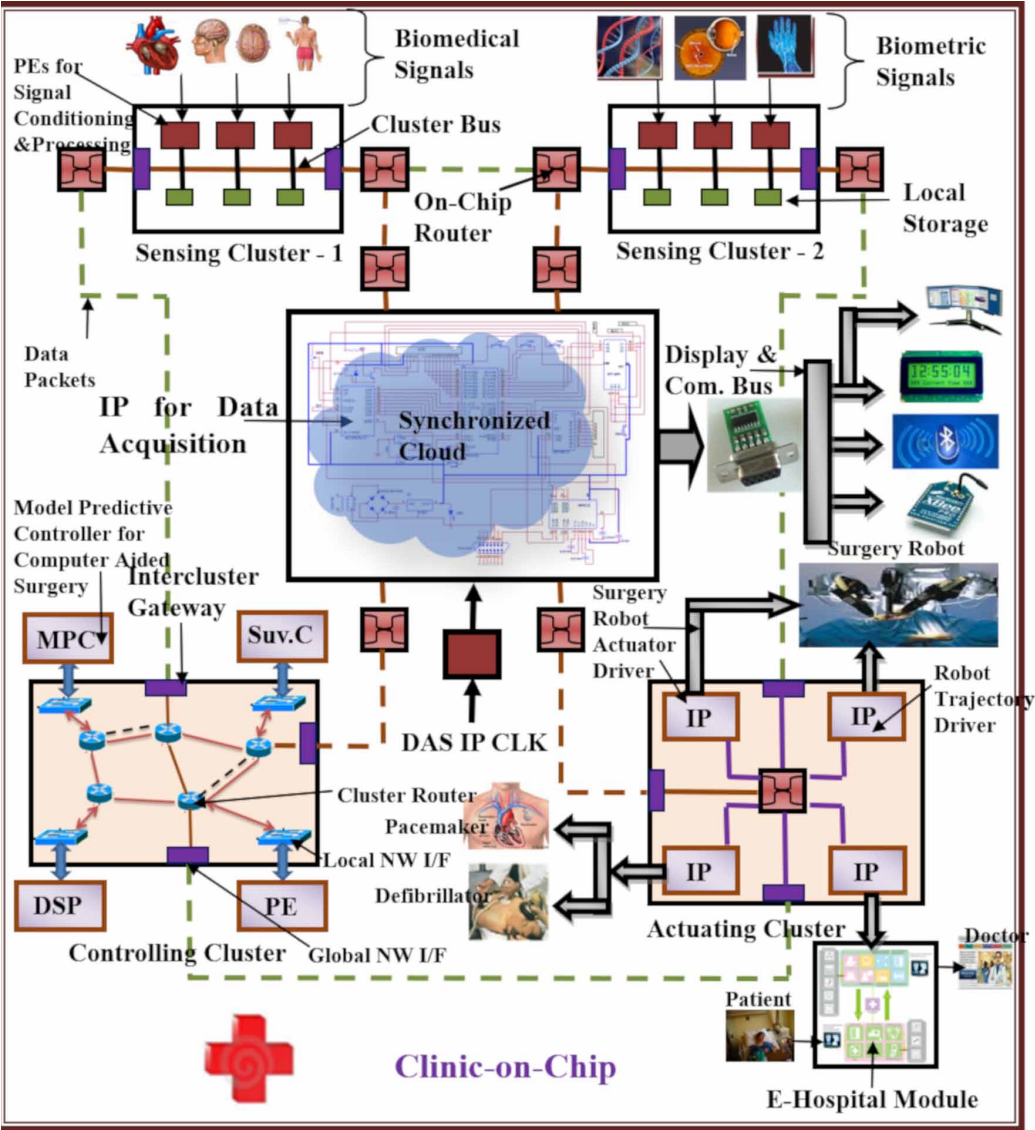


Figure 13. NoC implementation in e-hospital



## REFERENCES

- Saini, R. K., & Ahmed, M. (2015, January). 2D Hexagonal Mesh Vs 3D Mesh Network on Chip: A Performance Evaluation. *International Journal of Computing and Digital Systems*, 3(3), 33–41. doi:10.12785/ijcds/040104
- Kourdy, R., & Nouri, M.R. (2012). Performance Comparison of 2D and 3D Torus Network-on-Chip Architectures. *Journal of Computing*, 4(2), 119-122.
- Paulo, D., & Ababei, C. (2010). 3D network-on-chip architectures using homogeneous meshes and heterogeneous floorplans. *International Journal of Reconfigurable Computing*.
- Yan, S., & Lin, B. (2011). Design of application-specific 3D networks-on-chip architectures. *Proceedings of the 3D Integration for NoC-based SoC Architectures* (pp. 167-191). Springer.
- Matsutani, H., Koibuchi, M., & Amano, H. (2007, September). Tightly-coupled multi-layer topologies for 3-D NoCs. *Proceedings of the 2007 International Conference on Parallel Processing (ICPP 2007)* (pp. 75-75). IEEE.
- Dally, W. J., & Towles, B. (2001, June). Route packets, not wires: on-chip interconnection networks. *Proceedings of the 38th annual Design Automation Conference* (pp. 684-689). ACM.
- Ye, Y., Duan, L., Xu, J., Ouyang, J., Hung, M. K., & Xie, Y. (2009, September). 3D optical networks-on-chip (NoC) for multiprocessor systems-on-chip (MPSoC). *Proceedings of the 2009 IEEE International Conference on 3D System Integration* (pp. 1-6). IEEE. doi:10.1109/3DIC.2009.5306588
- Vasilis, F. P., & Friedman, E. G. (2007). 3-D topologies for networks-on-chip. *IEEE Transactions on Very Large Scale Integration Systems*, 15(10), 1081–1090.
- Beyne, E. (2006, April). 3D system integration technologies. *Proceedings of the 2006 International Symposium on VLSI Technology, Systems, and Applications* (pp. 1-9). IEEE.
- Bartzas, A., Skalis, N., Siozios, K., & Soudris, D. (2007, October). Exploration of alternative topologies for application-specific 3d networks-on-chip. In *Proc. of WASP* (Vol. 5, p. 43). Academic Press.
- Rahmani, A. M., Latif, K., Liljeberg, P., Plosila, J., & Tenhunen, H. (2010, November). Research and practices on 3D networks-on-chip architectures. [IEEE.]. *Proceedings of NORCHIP, 2010*, 1–6.
- Khan, M.A., & Ansari A.Q. (2011). A quadrant-XYZ routing algorithm for 3-D asymmetric torus network-on-chip. *The Research Bulletin of Jordan ACM*.
- Feero, B. S., & Pande, P. P. (2009). Networks-on-chip in a three-dimensional environment: A performance evaluation. *IEEE Transactions on Computers*, 58(1), 32–45. doi:10.1109/TC.2008.142
- Ogras, U. Y., Hu, J., & Marculescu, R. (2005, September). Key research problems in NoC design: a holistic perspective. *Proceedings of the 3rd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis* (pp. 69-74). ACM.
- Ahmed, A.B., & Abdallah, A.B. (2013). Architecture and design of high-throughput, low-latency, and fault-tolerant routing algorithm for 3D-network-on-chip (3D-NoC). *The Journal of Supercomputing*, 66(3), 1507–1532. doi:10.1007/s11227-013-0940-9
- Sehgal, V. K. (2015). Markovian models based stochastic communication in networks-in-package. *IEEE Transactions on Parallel and Distributed Systems*, 26(10), 2806–2821. doi:10.1109/TPDS.2014.2358218
- Al Khatib, I., Russo, G., & Nabiev, R. Performance analysis of interoperability protocols and algorithms in networks-on-chip for the next generation biomedical sensor-networks. *Proceedings of IEEE INFOCOM 2006* (pp. 23-29). IEEE Press.
- Wang, L., Yang, G. Z., Huang, J., Zhang, J., Yu, L., Nie, Z., & Cumming, D. R. (2010, April). A wireless biomedical signal interface system-on-chip for body sensor networks. *IEEE Transactions on Biomedical Circuits and Systems*, 4(2), 112–117. doi:10.1109/TBCAS.2009.2038228 PMID:23853318



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